REMARKS

Applicant respectfully thanks the Examiner for the courtesies extended during the personal interview on May 23, 2001. At that time, Applicant proposed "to submit claims drawn to the sequence of steps required or requiring the structure that is present during the FALC step." The Examiner stated that he would consider such claims.

In the final Office Action dated February 2, 2001, the Examiner rejected claims 1-36 under 35 U.S.C. § 103, as being unpatentable over the combination of Maekawa (US Patent No. 6,066,547), Arai et al. (US Patent No. 5,576,222) and Seung-Ik Jun (Aepse '97) and/or Cristoloveanu et al. (SOI).

At the outset, Applicant believes that Seung-Ik Jun is not an appropriate prior art. Regarding, Maekawa, Arai et al. and Cristoloveanu et al., Applicant respectfully submits that the claims, as amended, are allowable over these references, singly or in combination, and reconsideration is respectfully requested.

As shown above, Applicant has amended the claims, as suggested by the Examiner, to include that the substrate is a "glass" substrate and that "the thin film transistor having crystallized amorphous silicon layer is formed at each of the plurality of pixels" in combination with "crystallizing the amorphous silicon layer." As discussed during the Examiner interview, these cited references do not teach or suggest such combination of features of the claimed invention.

Moreover, both Arai et al. and Cristoloveanu et al. concern a high temperature process which would destroy the glass substrate of the claimed invention. For example, Arai et al. recites "producing an insulating layer on said solid phase growth layer by oxidizing surface of said solid

phase growth layer at temperature 900°C – 1100°C." Such high temperature would completely destroy the glass substrate, which would teach directly against using a glass material. Also, Cristoloveanu et al. concerns silicon-on-insulator (SOI) which is also a high temperature process.

In view of the foregoing, Applicant believes that this application is now in condition for allowance and therefore request favorable consideration and prompt allowance of the pending claims.

If the Examiner deems that a telephone conference would further the prosecution of this application, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0911.

Respectfully submitted,

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MARKED-UP VERSION OF THE CLAIMS

1. (Amended) A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising [the steps of]:

forming an amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a gate electrode on the amorphous silicon layer;

doping impurities of a first conductive type in the amorphous silicon layer;

forming a metal layer on the exposed portions of the amorphous silicon layer; and

crystallizing the amorphous silicon layer by applying thermal treatment and electric field to the resultant substrate,

wherein the thin film transistor having crystallized amorphous silicon layer is formed at each of the plurality of pixels.

14. (Amended) A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising [the steps of]:

forming a first amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a second amorphous silicon layer as a gate electrode on the first amorphous silicon layer;

doping impurities of a first conductive type in the first and second amorphous silicon layers;

forming a metal layer on the doped portions of the first and second amorphous silicon layers; and

crystallizing the first and second amorphous silicon layers by performing heat treatment and applying electric filed on the resultant substrate,

wherein the thin film transistor having crystallized amorphous silicon layer is formed at each of the plurality of pixels.

25. (Amended) A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising [the steps of]:

forming an amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a gate electrode on the amorphous silicon layer;

forming a metal layer on exposed portions of the amorphous silicon layer;

doping impurities of a first conductive type in the amorphous silicon layer after the metal layer is formed; and

crystallizing the amorphous silicon layer by applying thermal treatment and an electric field to the resultant substrate,

wherein the thin film transistor having crystallized amorphous silicon layer is formed at each of the plurality of pixels.